Resume of
Paul C. Teixeira

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Overview:

Innovative and hardworking verification engineer with 15 years of experience; interested in leading and developing verification methodologies using the most recent technology and tools. Always open to new areas of work and study.

Summary of Qualifications:

- ASIC verification technical lead – methodology, schedule, test plan, and execution
- RTL and Post-Si verification, architecture, development, and training for network processor ASICs, using knowledge of test bench methodology with System Verilog, UVM, VMM, NTB/Vera, & RVM
- Current use of Synopsys VCS, DVE, & Perl scripts, past usage of Debussy, Verisity Specman, Cadence nc suite, signalscan, virsim, and Xilinx
- Programming Languages – System Verilog, Vera, Verilog, TCL, e, C
  - Light Use – Perl, Ruby, C++, HTML
- Reliable, efficient and accurate; dedicated to quality results
- Work well with people of various backgrounds and ideas

Work Experience:

Cisco Systems, Inc. by Acquisition of Vihana, Inc., San Jose, CA
12/18/2003 – Present

Technical Lead, ASIC Design Verification –

- Technical project lead for full chip and Post-Si Verification effort of a 200Gbps NPU ASIC featuring packet processing, queuing, and scheduling. Lead test plan closure and execution for a team of 5 verification engineers. The environment is a combination of System Verilog with UVM, and C++.
- Design Verification Methodology Team for a Multi-ASIC routing project. Responsible for architecting, developing, training, and supporting a DV methodology with System Verilog & VMM1.2 for a large DV user base. Specialties include interrupt error handling, demo test bench, and test plan methodology.
- Architected and developed project wide Post-Si verification environment for 6 ASICs using a custom TCL tool suite with pre-production IOX-XR router software. Responsible for coding and supporting the environment for multiple users. Engaged with software team to provide custom hardware verification hooks for testing. Environment led to timely Post-Si validation of all ASICs despite hurdles with pre-production custom router software needs.
- Developed ASIC wide verification methodology using Vera and RVM for a new verification team working on an ingress packet shaper and packet to cell fabric interface ASIC for a 100Gbps router. Integrated RVM methodology with a modularized test bench structure, and functional coverage methodology, which allowed for entire verification team to quickly start building block level environments consistently and successfully. Developed all tool support scripts for simulation run, regression, test plan capture and functional coverage collection. Responsible for ASIC level verification effort and support of block level DV team.
- Verification lead for a Network Memory Processing Element super block. Test plan and coverage closure, as well as execution of interrupt and error conditions, and the processor's Arithmetic and custom network related operations.
- Owned the RTL verification effort for the DMA over PCI/PCI-X engine in a RegEx Processor ASIC. Completing the entire testplan development and successfully executing it before tapeout was the key contribution to enabling a bug-free DMA engine in 1st silicon. Developed the testplan, coverage goals, and schedule. Coded a self-checking directed/random testbench and PCI/PCI-X BFM. Achieved 100% functional and line coverage with this environment. Also responsible for verifying the entire DMA and PCI/PCI-X error handling and recovery procedures, including interrupt servicing.
- Sole Responsibility for the post-silicon compliance testing of the PCI/PCI-X 133 MHz interface. Completed compliance testing to both the PCI specification revision 2.3 and PCI-X specification revision 1.0b. Selection of VMETRO hardware tools, creation of testplan and schedule, and execution of all tests. Use of both the bus analyzer/exerciser and RTL testbench to test every PCI-SIG compliance checklist item.

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PMC-Sierra, Inc., Santa Clara, CA 8/16/1999 – 12/16/2003

Product Design/Verification Engineer, Micro-Processor & Optical Networking Divisions –

- Completed RTL verification of a DMA over Gigabit Ethernet block in a MIPS SOC chip. Specifically verified the interrupt based packet processing engine, descriptor and buffer management, and protocol error cases, as well as test case, test plan, and revision control management. Similar experience with designing and implementing a Specman and Verilog simulation environment for the E9000 MIPS CPU core with a proprietary transaction based interface.
- Post-Si validation of the ATLAS-II ATM traffic manager ASIC. Validation using a Compact-PCI station and TCL environment to test against the ATM standard for Fault Monitoring and Change of State FIFO Operation. TCL test programs were self-checking and interfaced to the PCI station, Windows, an Adtech traffic generator, and some proprietary FPGA traffic generation boards for controlling multi-phy and other traffic scenarios.
- Top Level Device Integration for the ATLAS-II and ARROW 2xGE ASICS. Completed JTAG/Scan verification, netlist generation, scripting, revision control, and interfacing with Layout and Product Engineering. The ATLAS-II was a 1.5 million gate, 64-Mbit Embedded DRAM, OC-48 ATM traffic manager chip, and was a Rev. A success. The ARROW2xGE was a 2 million gate Gigabit Ethernet over Sonet transport chip, and also a Rev. A success.
- Completed the entire design flow for the Backward Cell Interface in ATLAS-II. Implemented design, synthesis, and verification, as well as Scan Insertion and ATPG in the DFT flow. The interface was a UL2 to UL3 FIFO based converter running at 52 MHz UL2 side and 125 MHz UL3 side.
- Added TUG-3 SDH support to an existing 20K gate Sonet Transmit VC block for the ARROW 2xGE feature update ASIC.

IBM, San Jose, CA 6/29/1998 – 8/16/1999

Development Engineer for Test Engineering, Storage Systems Division –

- Completed the design, verification, production, debug, and documentation of a multi-speed motor control circuit board that reduced tester cost and improved motor control. Use of Xilinx Foundation software, and Xilinx FPGA's.
- Maintained, upgraded, and documented the hardware control software for a manufacturing line tester using C and a proprietary command interpreter as programming tools. Manufacturing line and clean room experience.
- Created and maintained a department Website running on Windows NT Workstation using IIS 4.0, perl for NT, MS Front Page, and MS Office.

Presentations:

- Chips @ Cisco 2009 - Functional Coverage for Verification with Verilog

Education:

- University of California, Davis, CA. *Bachelor of Science, Electrical Engineering* - Graduated June 19, 1998 with Highest Honors.

References Available upon Request